The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 37

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MELIK ISBARA

Appeal No. 2002-0397
Application 08/925,868[1]

ON BRIEF

Before BARRETT, RUGGIERO, and GROSS, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) from the rejection of claims 1-17, 19, and 20. Appellant limits the appeal to independent claims 1, 8, 13, 15, and 17.

We reverse.

[1] Application for patent filed September 9, 1997, entitled "Method and Apparatus for Interfacing Mixed Voltage Signals."

BACKGROUND

The invention relates to a method and apparatus for interfacing binary signals of different voltage levels.

Claim 1 is reproduced below.

1. An apparatus comprising:

a transistor having an enable terminal, an input terminal, and an output terminal, said input terminal coupled to receive binary signals that vary between first and second preselected voltage levels, and said output terminal coupled to deliver binary signals that vary between the first preselected voltage level and a third preselected voltage level;

a capacitor coupled across said input and output terminals of said transistor; and

a resistive element having a first end portion coupled to the enable terminal of said transistor and a second end portion coupled to a voltage supply to bias the transistor continuously on, the resistive element cooperating with a parasitic capacitor defined by said transistor to increase the voltage applied to the enable terminal during a transition from the first to the second preselected voltage level at the input terminal.

The examiner relies on the following references:

Nelson	4,507,618	March 26, 1985
Townley	4,970,478	November 13, 1990
Carroll	5,130,571	July 14, 1992
Ohmi et al. (Ohmi)	5,604,364	February 18, 1997
Storino et al. (Storino)[2]	6,111,422	August 29, 2000 (effective filing date December 7, 1995)
Ciraula et al. (Ciraula)	6,111,434	August 29, 2000 (filed July 21, 1997)

[2] Not listed in the prior art in the examiner's answer, page 3, but mentioned in the examiner's answer at page 5.

Claims 1, 8, 13, 15, and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nelson. Townley, Carroll, and Ohmi are cited to show the equivalence of a discrete resistor and a continuously-biased FET. Storino and Ciraula are cited to show that a half-latch was well known in the art.

In response to appellant's original appeal brief (Paper No. 30, January 16, 2001) (pages referred to as "Br__"), the examiner reopened prosecution to purportedly set forth a new ground of rejection (Paper No. 31, February 28, 2001). However, the rejection over Nelson was the same; the rejection referred to Carroll, Townley, Ohmi, Ciraula, and Storino (Paper No. 31, page 4), but did not incorporate them into the rejection. Appellant filed a supplemental appeal brief (Paper No. 32, received May 31, 2001) asserting that the rejection was improper because it contained no new ground of rejection and incorporated by reference the original appeal brief. The examiner entered an examiner's answer (Paper No. 33, August 16, 2001) (pages referred to as "EA__") and appellant filed a reply brief (Paper No. 34, October 22, 2001) (pages referred to as "RBr__").

OPINION

Claim 1 is selected as the representative claim.

The examiner finds that "Nelson discloses an RC attenuator, which is essentially all that appellant is reciting in this claim" (EA3). The examiner finds that the difference between

Nelson and the subject matter of claim 1 "is that appellant uses a continuously-on biased FET instead of the discrete resistor shown by [Nelson]" (EA3). The examiner reasons (EA3-4):

> [T]he replacement of a discrete resistor with a continuously-on biased FET is notoriously well-known in the art (official notice is taken) and there is obvious motivation to make such a replacement, i.e., to save chip real estate, since discrete resistors take up more space than integrated FETs acting as resistance element. The resistor recited in the claim also fails to distinguish patentably over Nelson because it is also old and well-known in the art to add such a series resistor between the gate bias voltage and the gate of the FET for the purpose of controlling the on level of the FET (and thereby controlling the resistance value of the FET), which is an old and well-known concept to those having ordinary skill in the art.

The examiner cites Carroll, Figs. 1 and 2, Townley, Figs. 3-6, and Ohmi, Fig. 9 as showing the equivalence between a discrete resistor and a continuously biased FET (EA5).

Appellant argues that the claimed biased transistor includes a parasitic capacitance and, therefore, is not structurally similar to an RC attenuator circuit using discrete resistors (Br6-7). It is argued that while a transistor, continuously biased ON, may provide impedance between its input and output terminals, e.g., resistance, unlike a discrete resistor, the transistor comprises a parasitic capacitance that cooperates with a resistive element coupled to the transistor's enable terminal to increase ("pump") the voltage applied to the enable terminal

during the transition from a first to a second binary voltage level (Br6). It is argued (Br6-7):

> In other words, unlike a discrete resistor, the transistor exhibits voltage "pumping" at the enable terminal to affect the impedance between the input and output terminals during a transition from the first to the second preselected voltage level at the input terminal.
>
> In fact, such "pumping" action is contrary to the "attenuation" produced by an RC attenuator, in that the effect of such pumping actually enhances signal propagation from input to output terminals. Attenuation, by contrast, involves the inhibition of signal propagation between terminals.

It is argued that Nelson and the claimed invention are not structurally the same because "the claimed circuit operates differently (using charge pumping), with a different effect (level shifting of a binary signal), using a different structure (a biased transistor instead of a discrete resistor)" (Br8). Appellant presents several additional arguments about the different operation and different structure (Br9).

The examiner responds that "the resistor/capacitor parallel combination of Nelson is an equivalent structure to appellant's constantly biased FET/capacitor parallel combination . . . [t]wo circuits that are structural equivalents can certainly be considered to be structurally similar" (EA6).

Nelson discloses an RC attenuator comprising essentially a voltage divider. Resistor R_1 and capacitor C_1 are connected in parallel in a series path and resistor R_2 and capacitor C_2 are connected in parallel in a shunt path (Fig. 3). The impedance of

R_1 and C_1 is Z_1 and the impedance of R_2 and C_2 is Z_2. The attenuation factor ATT = $Z_2/(Z_1 + Z_2)$ (col. 1 eqn. (1)), which is recognized as the voltage division expression. The attenuation factor ATT is frequency independent if $C_1R_1 = C_2R_2$ (col. 1, lines 44-47). However, it is often difficult to satisfy this relationship by manual adjustment. Nelson detects any incorrect frequency response at the output of the attenuator and electrically compensates for it (col. 2, lines 35-42). Nelson performs the claimed function of transforming "binary signals that vary between first and second preselected voltage levels" to "binary signals that vary between the first preselected voltage level and a third preselected voltage level." The output shown in Fig. 2B is attenuated from the input in Fig. 2A, where it is assumed that the lower (first) voltage level could be zero volts. However, Nelson does not perform the function using the structure and function of the claimed invention. Manifestly, there can be many patentable ways to perform the same function.

The examiner undertakes to perform a wholesale rebuilding of Nelson by taking Official Notice of the equivalence of resistors and biased FETs and then by adding in a gate resistor. There is certainly no suggestion for this modification in Nelson; indeed, since Nelson is an RC attenuator, structured as a voltage divider, and since the rejection appears to require replacing the RC attenuator 14 (not just one resistor) with an FET, the

modification would completely change Nelson. That is, the rejection requires doing more than replacing a fixed resistor with an active element FET acting as a resistor in a one-to-one swap; it requires replacing the voltage divider structure in Nelson (an RC impedance in series and an RC impedance in shunt) with a single FET. The examiner's rejection does not address this difference in structures or show that these structures were known to be equivalent. Furthermore, we agree with appellant's arguments that the claimed structure is different because a parasitic capacitor is not present in the RC attentuator of Nelson and an FET operates differently than the RC attenuator in Nelson because of the "pumping" effect of this parasitic capacitor. The examiner's rejection ignores the structural and operational differences stated in these arguments. The examiner states that "any resulting effect of the claimed structure will of course be present once the obvious modification of Nelson's Fig. 5 is made" (emphasis omitted) (EA7), which we interpret to mean that if the RC voltage divider attenuator 14 of Nelson is replaced with a biased FET, the parasitic capacitor and its function would be inherent. This idea of modifying a reference for one reason (replacing one kind of resistor with another kind of resistor) and then stating that other claimed structure and functions (parasitic capacitor and "pumping") would be inherent is indicative of hindsight based on appellant's disclosure. Such

a retrospective view of inherency is not a substitute for some teaching or suggestion supporting an obviousness rejection. See In re Newell, 891 F.2d 899, 901, 13 USPQ2d 1248, 1250 (Fed. Cir. 1989). The examiner has failed to show that a biased FET was a known equivalent in terms of structure and function to the RC attenuator constructed as a voltage divider in Nelson.

Appellant argues that the examiner's motivation, to save chip real estate, is erroneous since "the motivation to save chip real estate is not met by replacing a single resistor with a combination of a FET and gate bias resistor" (RBr5).

Of course, the examiner is not able to reply to an argument in the reply brief. Nevertheless, the examiner should have been able to anticipate an argument that replacing a single resistor with an FET and a resistor does not save parts or space. In addition, there appears to be no suggestion in the references that the circuit of Nelson is on a chip where chip real estate is a problem to be solved. Thus, the examiner appears to be inventing reasons to combine and we agree with appellant that the examiner's stated motivation is not persuasive.

Regarding Carroll, Townley, and Ohmi, appellant argues that "replacing a discrete resistor with a continuously-on biased FET is not notoriously well known in the art for all circuit applications" (RBr4). Appellant notes the different purposes of

the references and states that it would be improper to generalize from the narrow teachings of the references (RBr3-4).

Initially, we note that the rejection must contain a mention of all references applied in the rejection. See In re Hoch, 428 F.2d 1341, 1342 n.3, 166 USPQ 406, 407 n.3 (CCPA 1970); Ex parte Movva, 31 USPQ2d 1027, 1028 n.1 (Bd. Pat. App. & Int. 1993). Accord Ex parte Hiyamizu, 10 USPQ2d 1393, 1394 (Bd. Pat. App. & Int. 1988); In re Raske, 28 USPQ2d 1304, 1304-05 (Bd. Pat. App. & Int. 1993); MPEP § 706.02(j) (7th ed., rev. 1, Feb. 2000). The references should have been made part of the statement of the rejection. Nevertheless, we address the references because they are discussed by appellant. Carroll, Figs. 1 and 2, show that a transistor M1 can be thought of as an equivalent resistor R_{eq} (col. 1, lines 20-24). Townley, Fig. 5, shows that an FET can be modeled as an equivalent circuit of a parallel combination of a capacitor and a resistor (col. 5, lines 46-49) and states that "[v]arying the voltage between the gate and source varies the value of the resistance Rp, thereby providing variable attenuation for the artificial transmission line" (col. 5, lines 49-52). Ohmi, Fig. 9, shows that a turned-on MOS transistor 40 can be modeled as an equivalent resistance R_M (col. 21, line 62 to col. 22, line 1). None of these references shows that an FET is equivalent to an RC voltage divider attenuator. The references do not show a parasitic capacitor

between a drain and a gate, or the function of such a capacitor. Thus, the mere equivalence between a resistor and a biased FET does not address the equivalence between an RC voltage divider attenuator and an FET or the difference in function of an FET over an RC attenuator because of the parasitic capacitor.

For the reasons stated above, we conclude that the examiner has failed to establish a prima facie case of obviousness. The rejection of independent claims 1, 8, 13, 15, and 17 is reversed.

We appreciate that the claims are very broad. We agree with the examiner the limitations "coupled to receive binary signals that vary between first and second preselected voltage levels" and "coupled to deliver binary signals that vary between the first preselected voltage level and a third preselected voltage level" could be interpreted to be statements of intended use since no circuit for inputting first and second voltage levels is claimed. If the examiner found the claimed structure of a transistor, biasing resistor, and capacitor (the parasitic capacitor being inherent in all transistors), appellant would have to claim a new use for an old circuit as a process claim instead of an apparatus under 35 U.S.C. § 100(b). However, on the record before us, which has been created by the examiner, we do not find the claimed subject matter to be obvious.

CONCLUSION

The rejection of claims 1, 8, 13, 15, and 17 is reversed.

REVERSED

LEE E. BARRETT
Administrative Patent Judge

JOSEPH F. RUGGIERO
Administrative Patent Judge

ANITA PELLMAN GROSS
Administrative Patent Judge

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